125MHz Digitizer Firmware Description

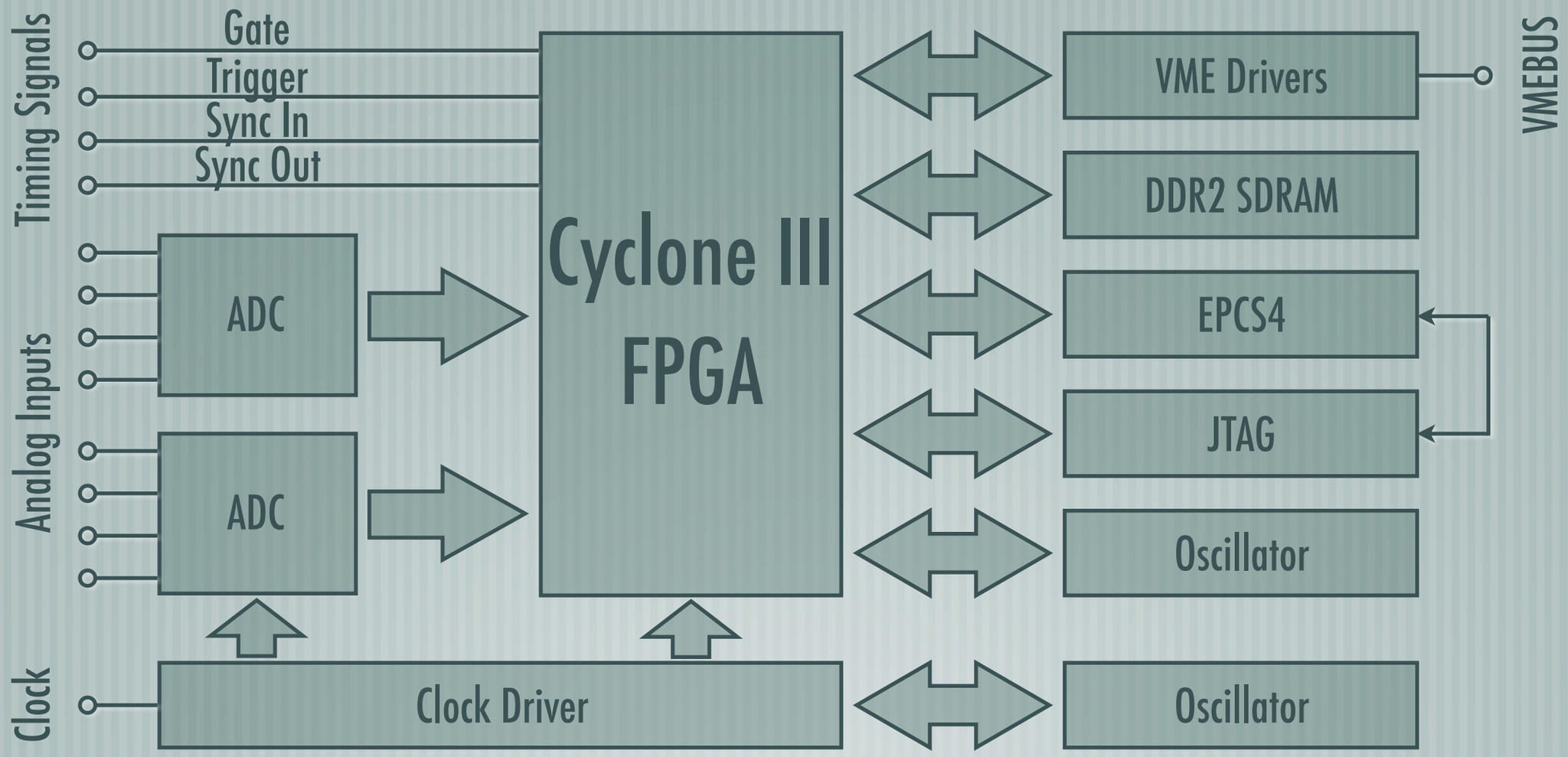
For Bunch By Bunch Toroid Intensity Monitors

Version: BBB07

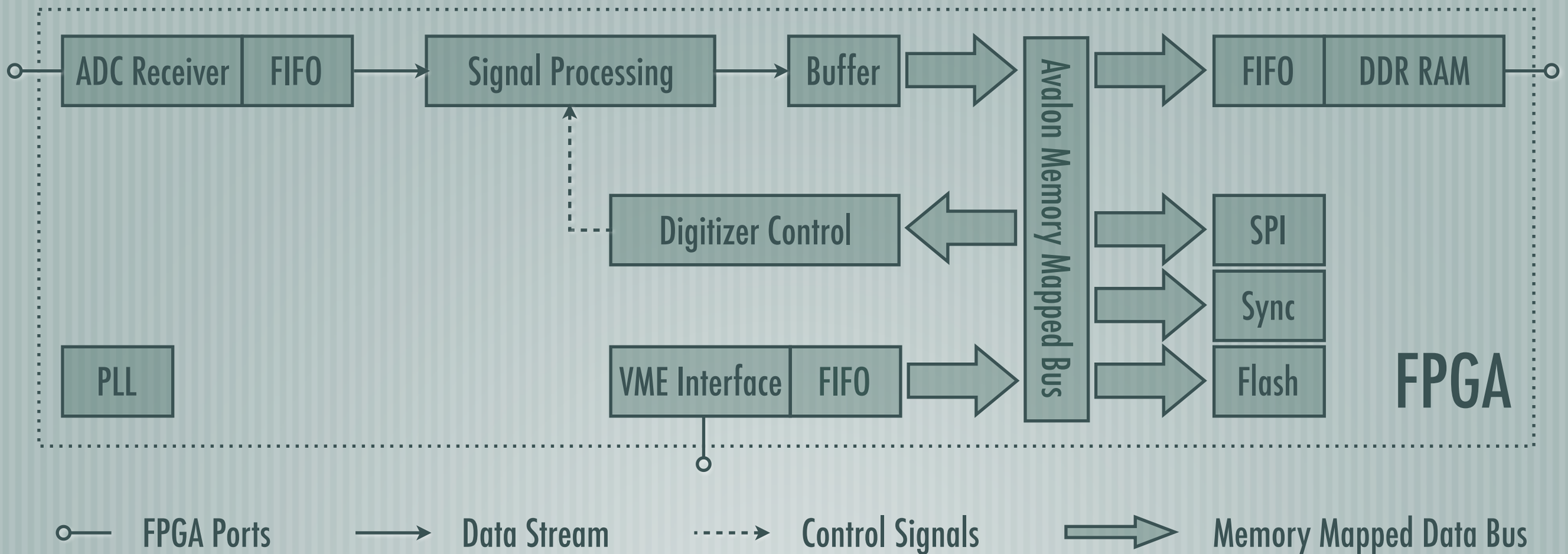
125 MHz Digitizer

- 6U VME Board
- 8 channels, 14 bit ADC @ 125MSPS
- DC coupling with ADS6445 Pre-Amp
- Hardware & software data processing
- 16M samples per channel buffer
- Smart triggering based on FPGA

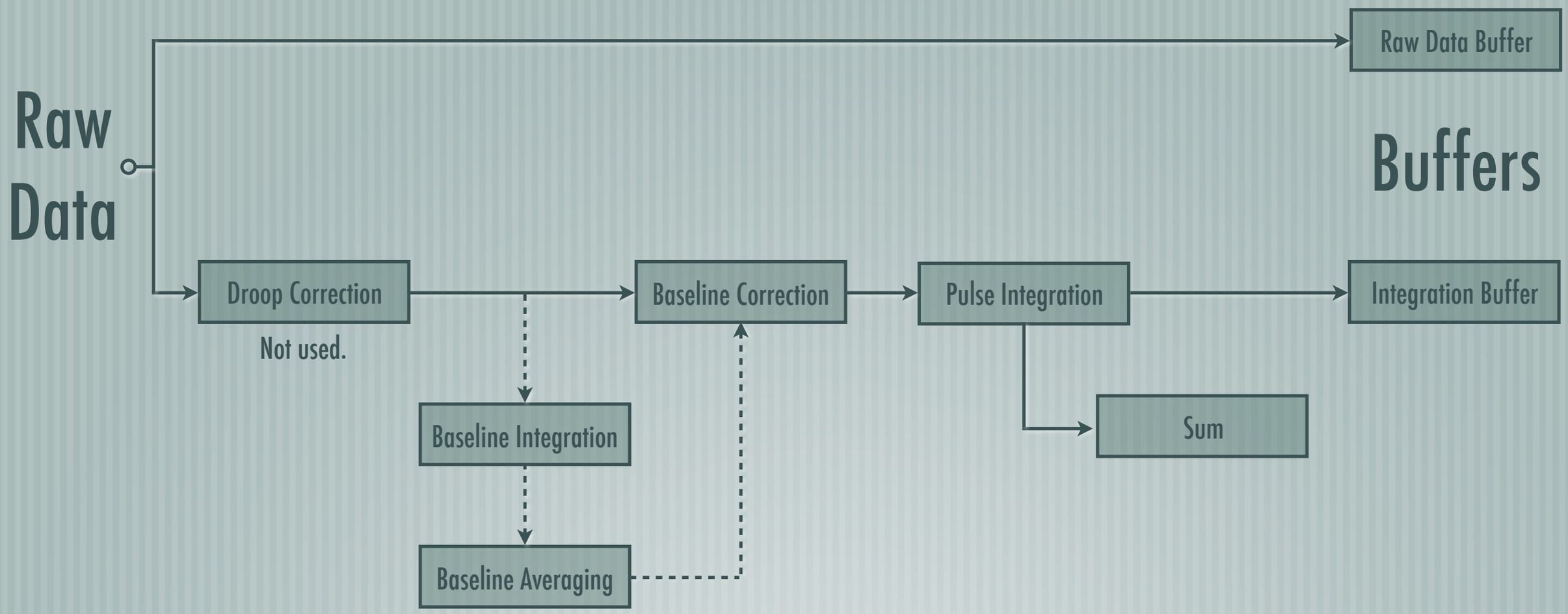
Digitizer Block Diagram



Firmware Structure

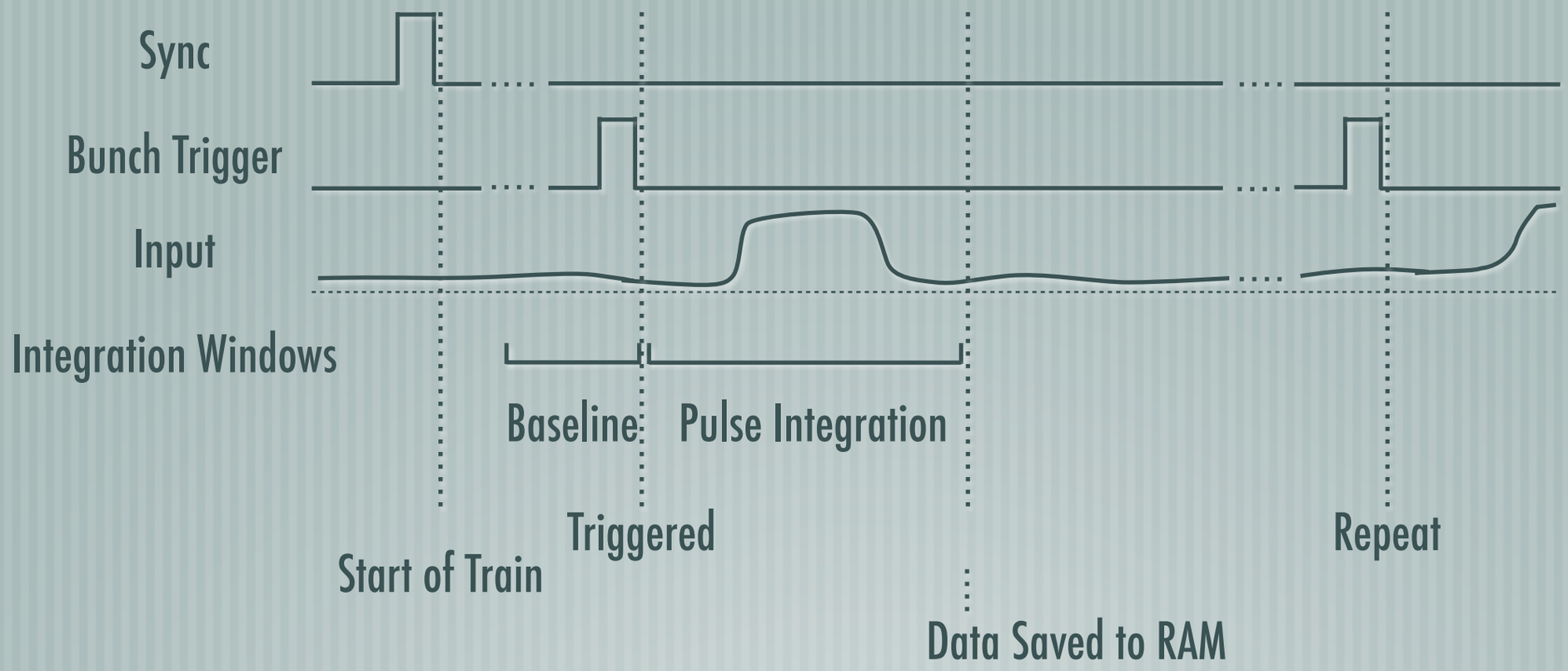


Signal Processing Diagram



Simplified data block diagram for each channel

Timing Diagram

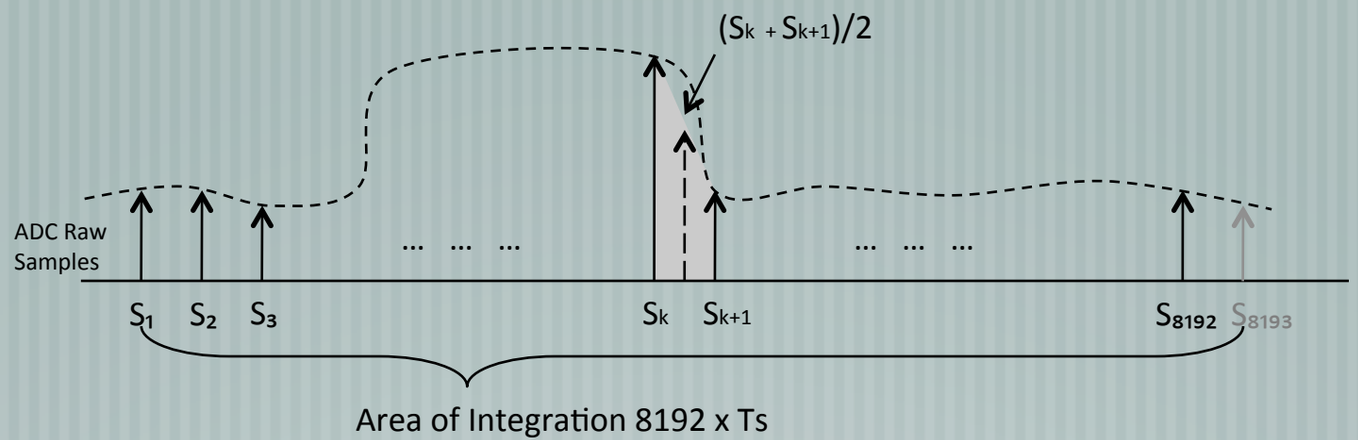


Stops operation after not receiving new trigger in 300 clock cycles.

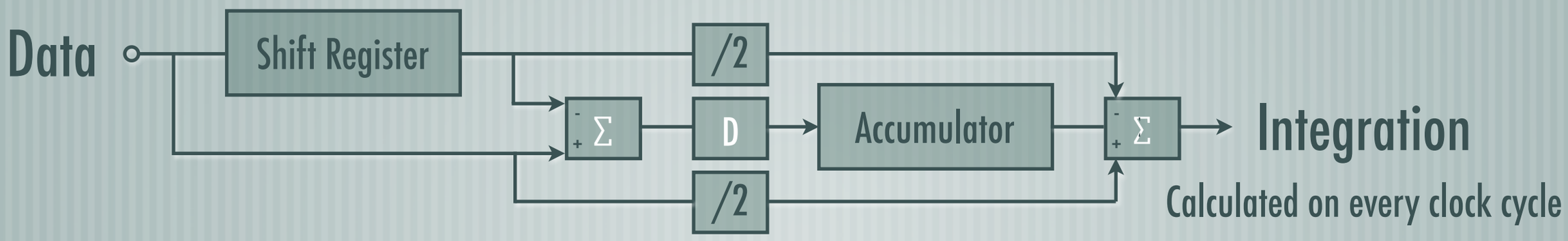
Note: RAM is overwritten at the beginning of each Sync

- Digitizer runs on internal clock at 125MHz or programmed clock in synchronization with RF.

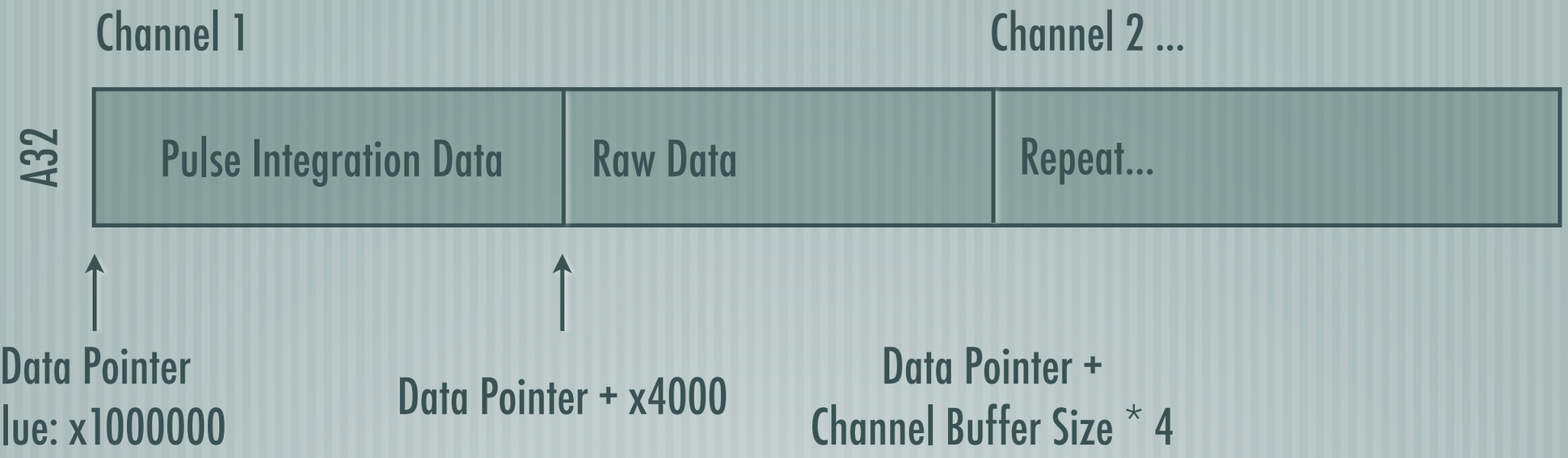
Trapezoidal Integration



$$\text{Int.}_{\text{Trapezoidal}} = \sum_{k=1}^{8192}\left(\frac{S_k + S_{k+1}}{2}\right) = \frac{S_1}{2} + \sum_{k=2}^{8192} S_k + \frac{S_{8193}}{2} = \sum_{k=1}^{8192} S_k + \frac{S_{8193}}{2} - \frac{S_1}{2}$$



Address Map



- Memory location for Integration data = Data Pointer + (CH# - 1) * Buffer Size * 4. For example, with default settings, channel 1 starts at x1000000, channel 2 at x1040000, etc.
- Raw data are stored in the channel's memory block after the corrected data. Address offset is x4000.
- All registers are in A16 address space with an offset set by the Hardware Address Switches. All addresses can be accessed in 8, 16 or 32 bits.

Key Registers (A16 space)

Register	Address (Hex)	Data Width	Default Value	Description
Digitizer Mode	HW + 200	8	x88	Use x88. Bit <7> - '1' - External (Sync) arm, '0' - software arm. Bit <6> - '1' - Sample on trigger, '0' - no trigger. Bit <5> - '1' - Use gate, '0' - no gate. Bits <3:2> - Use "10" for Integration mode.
Switch Off	HW + 201	8	x0	Write '1' to force digitizer to stop.
Software Arm	HW + 203	8	x0	Set to '1' to arm.
Digitizer Busy	HW + 2AE	8	x0	Read only. '1' - Busy, '0' - Not busy.
Firmware Version	HW + 2A8	32	xBBB07	Read only. Shows firmware version.
Block Count	HW + 218	32	x0	Read only. Number of runs.
A32 Data Pointer	HW + 04	32	x1000000	Address offset for corrected data. To access ADC raw data use Data Pointer + x4000 as address.
Channel Buffer Size	HW + 08	32	x10000	Number of 32-bit words reserved for each channel in the memory.
Raw Data Sampling Rate	HW + 204	16	x0	Bits <15:0> - Hex value is the sampling rate factor. Ts = Tmin * (Hex_Value + 1), where Tmin = 1 / clock_rate.
Number of Raw Samples	HW + 20C	32	x2000	Bits <23:0> - Number of samples or Number of Samples Per Trigger in trigger modes.

Key Registers Continued

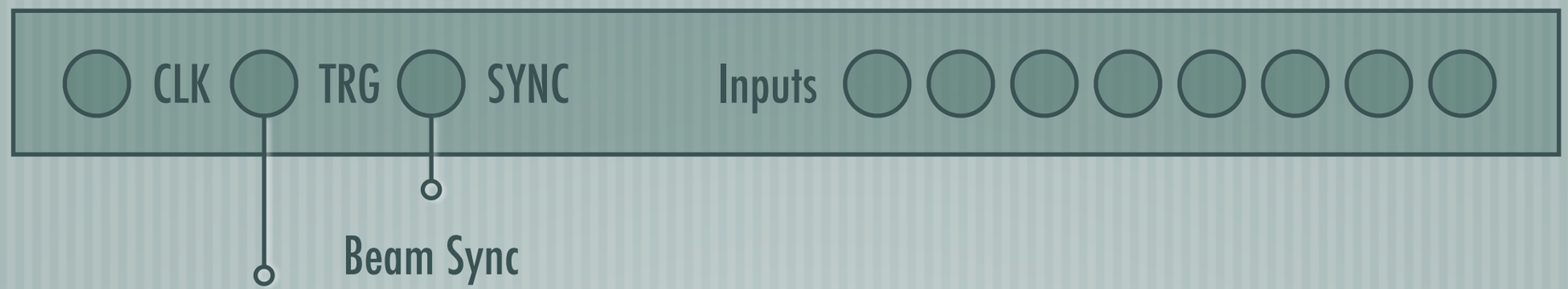
Register	Address (Hex)	Data Width	Default Value	Description
Trigger Delay	HW + 2B8	16	0x0	Delay of # of ADC-Clock cycles after receiving bunch trigger.
Window Size	HW + 2BA	16	0x20	Integration window size (in sample counts) for each bunch
Number of Bunches	HW + 2BC	16	0xBB8	Number of bunches to take.
Integration Gain	HW + 2BE	16	0xB	Bits <15:5>, unused. Bits <4:0> - Shifts Pulse Integration left by #. Then only the most significant 16 bit of the 32 bit integration are saved to memory. Gain = 2 ^ (# - 16).
Sync Delay	HW + 2C0	16	0x0	Delay of # ADC-clock cycles after digitizer is armed.
Pre-Trigger Delay	HW + 2C2	16	0x20	Delays the bunch trigger signal by # ADC-clock cycles. Do not modify.
Total Bunch Count	HW + 2C4	16	0x0	Read only. Total number of bunch triggers taken. Digitizer ends operation after not receiving new triggers for 300 clock cycles.

Register: Sums of All Pulses

Register	Address (Hex)	Data Width	Description
Sum Channel 1	HW + 3D0	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.
Sum Channel 2	HW + 3D4	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.
Sum Channel 3	HW + 3D8	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.
Sum Channel 4	HW + 3DC	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.
Sum Channel 5	HW + 3E0	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.
Sum Channel 6	HW + 3E4	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.
Sum Channel 7	HW + 3E8	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.
Sum Channel 8	HW + 3EC	32	Sum of integrations (16 bit, gain adjusted) of all triggered pulses in the train. Will count all the triggers regardless whether there is a pulse. Read only.

Connectors and Switches

Digitizer Front Panel



Hardware A16 Address Switches:

Registers: VME Interface

Register	Address	Data Width	Description
Channel Mask	0x00	8	Bits <7:0> - Set masks for Ch8 to Ch1 respectively. Bit <7> for Ch8, Bit <0> for Ch1. "1" = ON, "0" = OFF. Example: "00000001" means only Ch1 active.
DCDC Mode	0x01	8	Bits <1,0> - "00" – Fixed frequency; "01" – sweep 10% frequency; "1X" – spread spectrum. Default = "00".
VME IRQ Interrupt Level	0x02	8	Bits <2:0> - Hex number indicates the VME IRQ line. "000" = No interrupt "001" = IRQ1,"002" = IRQ2, ...
A32 Pointer for Raw Data	0x04	32	Indicates the starting address for ADC raw data in the A32 address space.
Channel Buffer Size for Raw Data	0x08	32	Indicates number of 32-bit words (two samples in each word) in memory reserved for each channel.
A32 Pointer for I/Q Data	0x0C	32	Indicates the starting address in memory for narrow band I and Q data.
Buffer Size for I/Q Data	0x10	32	Indicates number of 32-bit words in memory reserved for each channel.
A32 Pointer for Phase and Mag Data	0x14	32	Indicates the starting address in memory for narrow band phase and magnitude data.
Buffer Size for Phase and Mag Data	0x18	32	Indicates number of 32-bit words in memory reserved for each channel.
A24 Pointer for FPGA Flash Config Data	0x24	32	
Buffer Size for FPGA Flash Config Data	0x28	32	Indicates number of 32-bit words in memory reserved for each channel.
A24 Pointer for Flash Settings Data	0x2C	32	
Buffer Size for Flash Settings Data	0x30	32	Indicates number of 32-bit words in memory reserved for each channel.
VME A24 Pointer for Flash Data	0x34	32	
Buffer Size for Flash Data	0x38	32	Indicates number of 32-bit words in memory reserved for each channel.
Board ID (Read Only)	0x3C	32	Board ID, read only.

Registers: Interrupt

Register	Address	Data Width	Description
Software Set IRQ, #0 ~ #15	0x206	16	Bits <15:0> - IRQ15 ~ IRQ0. IRQ15 ~ IRQ12 not used in this design. Generate software interrupts by writing into register. Read back to see non-masked active interrupts (software or hardware generated).
VME IRQ Mask	0x290	16	Bits <11:0> - Mask for IRQ11 ~ IRQ0. "1" = Active, "0" = Disabled
IRQ Vector for IRQ #0	0x220	16	Active when ADC data out of range (any channel).
IRQ Vector for IRQ #1	0x222	16	Unassigned.
IRQ Vector for IRQ #2	0x224	16	Unassigned.
IRQ Vector for IRQ #3	0x226	16	Unassigned.
IRQ Vector for IRQ #4	0x228	16	Unassigned.
IRQ Vector for IRQ #5	0x22A	16	Unassigned.
IRQ Vector for IRQ #6	0x22C	16	Unassigned.
IRQ Vector for IRQ #7	0x22E	16	Unassigned.
IRQ Vector for IRQ #8	0x230	16	Unassigned.
IRQ Vector for IRQ #9	0x232	16	Unassigned.
IRQ Vector for IRQ #10	0x234	16	Active at start of digitizer mode
IRQ Vector for IRQ #11	0x236	16	Active at end of digitizer mode

Registers: ADC Overflow

Register	Address	Data Width	Description
ADC's OVR Status	0x2AD	8	Bits <7:0> - Denotes ADC data saturation for channels 8 to 1. Example: Bit <7> = Ch8. "1" = Overflow, "0" = Normal.
ADC 1 Abs Max Count	0x370	16	ADC data max count recorder for channel 1.
ADC 2 Abs Max Count	0x372	16	ADC data max count recorder for channel 2.
ADC 3 Abs Max Count	0x374	16	ADC data max count recorder for channel 3.
ADC 4 Abs Max Count	0x376	16	ADC data max count recorder for channel 4.
ADC 5 Abs Max Count	0x378	16	ADC data max count recorder for channel 5.
ADC 6 Abs Max Count	0x37A	16	ADC data max count recorder for channel 6.
ADC 7 Abs Max Count	0x37C	16	ADC data max count recorder for channel 7.
ADC 8 Abs Max Count	0x37E	16	ADC data max count recorder for channel 8.

Registers: ADC Delays

Register	Address	Data Width	Description
ADC 1 Data Delay	0x140	8	Bits <4:0> - Data delay for channel 1, in ADC samples. Ranges from “0” to “31”. Default is 16.
ADC 2 Data Delay	0x141	8	Bits <4:0> - Data delay for channel 2, in ADC samples. Ranges from “0” to “31”. Default is 16.
ADC 3 Data Delay	0x142	8	Bits <4:0> - Data delay for channel 3, in ADC samples. Ranges from “0” to “31”. Default is 16.
ADC 4 Data Delay	0x143	8	Bits <4:0> - Data delay for channel 4, in ADC samples. Ranges from “0” to “31”. Default is 16.
ADC 5 Data Delay	0x144	8	Bits <4:0> - Data delay for channel 5, in ADC samples. Ranges from “0” to “31”. Default is 16.
ADC 6 Data Delay	0x145	8	Bits <4:0> - Data delay for channel 6, in ADC samples. Ranges from “0” to “31”. Default is 16.
ADC 7 Data Delay	0x146	8	Bits <4:0> - Data delay for channel 7, in ADC samples. Ranges from “0” to “31”. Default is 16.
ADC 8 Data Delay	0x147	8	Bits <4:0> - Data delay for channel 8, in ADC samples. Ranges from “0” to “31”. Default is 16.

Registers: Sync Module

Register	Address	Data Width	Description
Time Stamp Counter	0x100	16	Read only. Sync with TCLK events. Bits <15:0> - Read back of time stamp counter.
TCLK Start Delay	0x102	16	Bits <15:0> - TCLK Start Delay.
TCLK Stop Delay	0x104	16	Bits <15:0> - TCLK Stop Delay.
TCLK Delay Scale	0x106	16	Bits <15:0> - TCLK Delay Scale.
BSYNC Start Delay	0x108	16	Bits <15:0> - BSYNC Start Delay.
BSYINC Stop Delay	0x10A	16	Bits <15:0> - BSYNC Stop Delay.
BSYNC Delay Scale	0x10C	16	Bits <15:0> - BSYNC Delay Scale.
TCLK Start Event	0x10E	8	Bits <7:0> - TCLK Start Event.
TCLK Stop Event	0x10F	8	Bits <7:0> - TCLK Stop Event.
BSYNC Start Event	0x110	8	Bits <7:0> - BSYNC Start Event.
BSYNC Stop Event	0x111	8	Bits <7:0> - BSYNC Stop Event.
SYNC In Source Mode	0x112	8	Bits <7:0> - Source for SYNC In signal. “0x0” = External Sync Signal, “0x1” = TCLK Start Event, “0x2” = TCLK Stop Event, “0x3” = BSYNC Start Event, “0x4” = BSYNC Stop Event.
Trigger Source Mode	0x113	8	Bits <7:0> - Source for Trigger signal. “0x0” = External Trigger Signal, “0x1” = TCLK Start Event, “0x2” = TCLK Stop Event, “0x3” = BSYNC Start Event, “0x4” = BSYNC Stop Event.
Gate Source Mode	0x114	8	Bits <7:0> - Source for Gate signal. “0x0” = External Gate Signal, “0x1” = TCLK Start/Stop Event, “0x2” = BSYNC Start/Stop Event.
SYNC Out Source Mode	0x115	8	Bits <7:0> - Source for Sync Out port. “0x0” = External Sync In, “0x1” = External Trigger, “0x2” = External Gate, “0x3” = TCLK Start Event, “0x4” = TCLK Stop Event, “0x5” = BSYNC Start Event, “0x6” = BSYNC Stop Event, “0x7” = ADC samples, “0x8” = Mode Active, “0x9” = ADC’s clock, “0xA” = ATF-NB gate, “0xB” = ATF-WB gates, “0xC” = BLM Alarm square wave, “0xD” = Turn Marker.

Registers: Sync IRQ

Register	Address	Data Width	Description
SYNC IRQ Mask	0x118	16	Bits <8:0> - Mask for SYNC IRQ8 ~ IRQ0. "1" = Active, "0" = Disabled
Software Set SYNC IRQ	0x11A	16	Bits <15:0> - SYNC IRQ15 ~ IRQ0. IRQ15 ~ IRQ9 not used in this design. Generate software interrupts by writing into register. Read back to see non-masked active interrupts (software or hardware generated).
IRQ Vector for IRQ #0	0x120	16	Active on external Sync Signal.
IRQ Vector for IRQ #1	0x122	16	Active on external Trigger signal.
IRQ Vector for IRQ #2	0x124	16	Active on external Gate signal positive edge.
IRQ Vector for IRQ #3	0x126	16	Active on external Gate signal negative edge.
IRQ Vector for IRQ #4	0x128	16	Active on TCLK Start event.
IRQ Vector for IRQ #5	0x12A	16	Active on TCLK Stop event.
IRQ Vector for IRQ #6	0x12C	16	Active on BSYNC Start event.
IRQ Vector for IRQ #7	0x12E	16	Active on BSYNC Stop event.
IRQ Vector for IRQ #8	0x130	16	Active on TCLK time stamp counter reset.

Registers: ADC Chip 1

Register	Address	Data Width	Description
Power Down Modes Reg. A	0x80	16	Bits <9:6> - Not Used. Must be “0”. Bit <10> - Software Reset. “1” resets all internal registers and self-clears to “0”. Bit <5> - Reference. “0”=Internal Reference Enabled, “1”=External Reference Enabled. Bits <4:1> - Channels 4~1 Power Down. “1”=Power Down, “0”=Normal Operation. Bit <0> - Global Power Down, including channels 1~4. “1”=Power Down, “0”=Normal Operation.
Input Clock Gain Reg. B	0x82	16	Bits <10:7, 1:0> - Not Used. Must be “0”. Bits <6:2> - CLKIN Gain. “11000”= Gain 0, minimum gain, “00000”= Gain 1, default gain after reset, “01100”= Gain 2, “01010”= Gain 3, “01001”= Gain 4, “01000”= Gain 5, maximum gain.
Capture Test Pattern Reg. C	0x84	16	Bits <10, 8, 4:0> - Not Used. Must be “0”. Bit <9> - Data Format Selection. “0” = 2’s Complement format, “1” = Straight binary format Bits <7:5> - Capture Test Patterns. “000”= Normal ADC operation, “001”= Output all zeros, “010”= Output all ones, “011”= Output toggle pattern, “100”= Unused, “101”= Output custom pattern (contents of CUSTOM pattern registers 0x86 and 0x88), “110”= Output DESKEW pattern (serial stream of 1010...), “111”= Output SYNC pattern.
Test Patterns Reg. D	0x86	16	Bits <10:0> - Lower 11 bits of custom pattern. “D10 D9 D8 ... D0”
Fine Gain Reg. E	0x88	16	Bits <2:0> - Upper 3 bits of custom pattern, “D13 D12 D11”. Bits <7:3> - Not Used. Must be “0”. Bits <10:8> - Fine Gain Control. “000”= 0dB Gain (full-scale range=2.00VPP), “001”= 1dB Gain (full-scale range=1.78VPP), “010”= 2dB Gain (full-scale range=1.59VPP), “011”= 3dB Gain (full-scale range=1.42VPP), “100”= 4dB Gain (full-scale range=1.26VPP), “101”= 5dB Gain (full-scale range=1.12VPP), “110”= 6dB Gain (full-scale range=1.00VPP).

Registers: ADC Chip 1 cont.

Register	Address	Data Width	Description
Output Data Config. Reg. F	0x8A	16	Bit <10> - Over-Ride Bit. All the functions in this register can also be controlled using the parallel control pins. By setting this bit to "1", the contents of register will over-ride the settings of the parallel pins. Bits <9:8, 3> - Not Used. Must be "0". Bit <7> - Byte/bit Wise outputs. "0": Byte wise, "1": bit wise. Bit <6> - MSB or LSB First Selection. "0": MSB First, "1": LSB First. Bit <5> - Coarse Gain Control. "0"=0dB Coarse Gain (full-scale range=2.0 VPP), "1"=3.5dB Coarse Gain (full-scale range=1.34 VPP) Bit <4> - Bit Clock Capture Edge (only when SDR bit clock is selected, Bit 1 = "1"). "0"=Capture data with falling edge of bit clock, "1"=Capture data with rising edge of bit clock. Bit <2> - Serialization Factor Selection. "0"=14x Serialization, "1"=16x Serialization. Bit <1> - Bit Clock Selection (only in 2-wire interface). "0"=DDR Bit Clock, "1"=SDR Bit Clock. Bit <0> - Interface Selection. "0"=1 Wire interface, "1"=2 Wire interface.
Data Interface Reg. G	0x8C	16	Bit <0> - LVDS Current Double For Data Outputs. "0"=Nominal LVDS current, as set by Bits <5:2>. "1"=Double the nominal value. Bit <1> - LVDS Current Double for Bit and Word Clock Outputs. "0"=Nominal LVDS current, as set by Bits<5:2>. "1"=Double the nominal value. Bits <3:2> - LVDS Current Setting for Data Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA; Bits <5:4> - CVDS Current Setting For Bit and Word Clock Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA; Bits <10:6> - LVDS Internal Termination For Bit and Word Clock outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010"= 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω; Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166 | | 250=100 Ω. "00101"= 100 Ω
Data Interface Reg. H	0x8E	16	Bits <10:9> - Only when 2-wire interface is selected. "00" Byte-wise or bitwise output, 1x frame clock, "11" Word-wise output enabled, 0.5x frame clock. Bits <8:5> - Not Used. Must be "0". Bits <4:0> - LVDS Internal Termination For Data Outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010", 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166 | | 250=100 Ω, "00101"= 100 Ω

Registers: ADC Chip 2

Register	Address	Data Width	Description
Power Down Modes Reg. A	0x90	16	Bits <9:6> - Not Used. Must be “0”. Bit <10> - Software Reset. “1” resets all internal registers and self-clears to “0”. Bit <5> - Reference. “0”=Internal Reference Enabled, “1”=External Reference Enabled. Bits <4:1> - Channels 4~1 Power Down. “1”=Power Down, “0”=Normal Operation. Bit <0> - Global Power Down, including channels 1~4. “1”=Power Down, “0”=Normal Operation.
Input Clock Gain Reg. B	0x92	16	Bits <10:7, 1:0> - Not Used. Must be “0”. Bits <6:2> - CLKIN Gain. “11000”= Gain 0, minimum gain, “00000”= Gain 1, default gain after reset, “01100”= Gain 2, “01010”= Gain 3, “01001”= Gain 4, “01000”= Gain 5, maximum gain.
Capture Test Pattern Reg. C	0x94	16	Bits <10, 8, 4:0> - Not Used. Must be “0”. Bit <9> - Data Format Selection. “0” = 2’s Complement format, “1” = Straight binary format Bits <7:5> - Capture Test Patterns. “000”= Normal ADC operation, “001”= Output all zeros, “010”= Output all ones, “011”= Output toggle pattern, “100”= Unused, “101”= Output custom pattern (contents of CUSTOM pattern registers 0x96 and 0x98), “110”= Output DESKEW pattern (serial stream of 1010...), “111”= Output SYNC pattern.
Test Patterns Reg. D	0x96	16	Bits <10:0> - Lower 11 bits of custom pattern. “D10 D9 D8 ... D0”
Fine Gain Reg. E	0x98	16	Bits <2:0> - Upper 3 bits of custom pattern, “D13 D12 D11”. Bits <7:3> - Not Used. Must be “0”. Bits <10:8> - Fine Gain Control. “000”= 0dB Gain (full-scale range=2.00VPP), “001”= 1dB Gain (full-scale range=1.78VPP), “010”= 2dB Gain (full-scale range=1.59VPP), “011”= 3dB Gain (full-scale range=1.42VPP), “100”= 4dB Gain (full-scale range=1.26VPP), “101”= 5dB Gain (full-scale range=1.12VPP), “110”= 6dB Gain (full-scale range=1.00VPP).

Registers: ADC Chip 2 cont.

Register	Address	Data Width	Description
Output Data Config. Reg. F	0x9A	16	Bit <10> - Over-Ride Bit. All the functions in this register can also be controlled using the parallel control pins. By setting this bit to "1", the contents of register will over-ride the settings of the parallel pins. Bits <9:8, 3> - Not Used. Must be "0". Bit <7> - Byte/bit Wise outputs. "0": Byte wise, "1": bit wise. Bit <6> - MSB or LSB First Selection. "0": MSB First, "1": LSB First. Bit <5> - Coarse Gain Control. "0"=0dB Coarse Gain (full-scale range=2.0 VPP), "1"=3.5dB Coarse Gain (full-scale range=1.34 VPP) Bit <4> - Bit Clock Capture Edge (only when SDR bit clock is selected, Bit 1 = "1"). "0"=Capture data with falling edge of bit clock, "1"=Capture data with rising edge of bit clock. Bit <2> - Serialization Factor Selection. "0"=14x Serialization, "1"=16x Serialization. Bit <1> - Bit Clock Selection (only in 2-wire interface). "0"=DDR Bit Clock, "1"=SDR Bit Clock. Bit <0> - Interface Selection. "0"=1 Wire interface, "1"=2 Wire interface.
Data Interface Reg. G	0x9C	16	Bit <0> - LVDS Current Double For Data Outputs. "0"=Nominal LVDS current, as set by Bits <5:2>. "1"=Double the nominal value. Bit <1> - LVDS Current Double for Bit and Word Clock Outputs. "0"=Nominal LVDS current, as set by Bits<5:2>. "1"=Double the nominal value. Bits <3:2> - LVDS Current Setting for Data Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA; Bits <5:4> - CVDS Current Setting For Bit and Word Clock Outputs. "00"= 3.5mA, "01"= 4mA, "10"= 2.5mA, "11"= 3mA; Bits <10:6> - LVDS Internal Termination For Bit and Word Clock outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010"= 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω; Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166 | | 250=100 Ω. "00101"= 100 Ω
Data Interface Reg. H	0x9E	16	Bits <10:9> - Only when 2-wire interface is selected. "00" Byte-wise or bitwise output, 1x frame clock, "11" Word-wise output enabled, 0.5x frame clock. Bits <8:5> - Not Used. Must be "0". Bits <4:0> - LVDS Internal Termination For Data Outputs. "00000"= No internal termination, "00001"= 166 Ω, "00010", 200 Ω, "00100"= 250 Ω, "01000"= 333 Ω, "10000"= 500 Ω Any combination of above bits can be programmed, resulting in a parallel combination of the selected values. For example, "00101" is the parallel combination of 166 | | 250=100 Ω, "00101"= 100 Ω

Registers: Clock Driver

Register	Address	Data Width	Description
Control Register 0 (Output Divider 0)	0xA0	32	Bits <0:1> - Pre-Divider selection for primary reference. “00” = 3-state, “01” = divide by 1, “10”, divide by 2, “11” = reserved. Bits <4:5> - Output Mux 0 Select. “00” = PRI_IN (On board oscillator), “01” = SEC_IN (External clock), “10” = SMART_MUX, “11” = VCO_CORE. Bits <12:6> - Coarse phase adjust select for output 0. Bits <19:13> - Output Divider 0 Ratio Select. Bit <20> - “1” = output 0 enabled, “0” = disabled. Bit <21> - High swing LVPEC when set to “1”, normal swing when set to “0”. Bits <3:2> - Reserved. Bits <26:27> - Output buffer select 0. Bits <22:23> - LVCMOS mode select for Output 0 positive pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state. Bits <24:25> - LVCMOS mode select for Output 0 negative pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state.
Control Register 1 (Output Divider 1)	0xA4	32	Bits <0:1> - Pre-Divider selection for secondary reference. “00” = 3-state, “01” = divide by 1, “10”, divide by 2, “11” = reserved. Bits <4:5> - Output Mux 1 Select. “00” = PRI_IN (On board oscillator), “01” = SEC_IN (External clock), “10” = SMART_MUX, “11” = VCO_CORE. Bits <12:6> - Coarse phase adjust select for output 1. Bits <19:13> - Output Divider 1 Ratio Select. Bit <20> - “1” = output 1 enabled, “0” = disabled. Bit <21> - High swing LVPEC when set to “1”, normal swing when set to “0”. Bits <3:2> - Reserved. Bits <26:27> - Output buffer select 1. Bits <22:23> - LVCMOS mode select for Output 1 positive pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state. Bits <24:25> - LVCMOS mode select for Output 1 negative pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state.
Control Register 2 (Output Divider 2)	0xA8	32	Bit<0> - Reference divider bit 0. Bit<1> - Reference divider bit 1. Bits <3:2> - Reserved. Bits <26:27> - Output buffer select 2. Bits <4:5> - Output Mux 2 Select. “00” = PRI_IN (On board oscillator), “01” = SEC_IN (External clock), “10” = SMART_MUX, “11” = VCO_CORE. Bits <12:6> - Coarse phase adjust select for output 2. Bits <19:13> - Output Divider 2 Ratio Select. Bit <20> - “1” = output 2 enabled, “0” = disabled. Bit <21> - High swing LVPEC when set to “1”, normal swing when set to “0”. Bits <22:23> - LVCMOS mode select for Output 2 positive pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state. Bits <24:25> - LVCMOS mode select for Output 2 negative pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state.
Control Register 3 (Output Divider 3)	0xAC	32	Bit<0> - Reference divider bit 2. Bits <3:1> - Reserved. Bits <26:27> - Output buffer select 3. Bits <4:5> - Output Mux 3 Select. “00” = PRI_IN (On board oscillator), “01” = SEC_IN (External clock), “10” = SMART_MUX, “11” = VCO_CORE. Bits <12:6> - Coarse phase adjust select for output 3. Bits <19:13> - Output Divider 3 Ratio Select. Bit <20> - “1” = output 3 enabled, “0” = disabled. Bit <21> - High swing LVPEC when set to “1”, normal swing when set to “0”. Bits <22:23> - LVCMOS mode select for Output 3 positive pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state. Bits <24:25> - LVCMOS mode select for Output 3 negative pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state.

Registers: Clock Driver cont.

Register	Address	Data Width	Description
Control Register 4 (Output Divider 4)	0xB0	32	Bit<0> - Reserved, must be set to “1”. Bits <3:1> - Reserved. Bits <4:5> - Output Mux 4 Select. “00” = PRI_IN (On board oscillator), “01” = SEC_IN (External clock), “10” = SMART_MUX, “11” = VCO_CORE. Bits <12:6> - Coarse phase adjust select for output 4. Bits <19:13> - Output Divider 4 Ratio Select. Bit <20> - “1” = output 4 enabled, “0” = disabled. Bit <21> - High swing LVPEC when set to “1”, normal swing when set to “0”. Bits <26:27> - Output buffer select 4. Bits <22:23> - LVCMOS mode select for Output 4 positive pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state. Bits <24:25> - LVCMOS mode select for Output 4 negative pin. “00” = Active, “10” = Inverting, “11” = Low, “01” = 3-state.
Control Register 5	0xB4	32	Bits <0:1> - Input buffer select. “01” = LVPECL, “11” = LVDS, “00” = LVCMOS. Bits <2:4> - EEPROM clock select. Bit <5> - EEPROM clock select enable. Bit <6> - Input buffer termination. “1” = DC, “0” = AC. Bit <7> - Input buffers hysteresis enable, “1” recommended. Bit <8> - Primary input termination. “0” = enable, “1” = disable. Bit <9> - Primary input negative pin biased with internal Vbb voltage when set to “1”. Bit <10> - Secondary input negative pin biased with internal Vbb voltage when set to “1”. Bits <13:12> - Reserved, must be “0”. Bit <11> - Fail Safe is enabled for all input buffers when set to “1”, DC coupling only. Bits <21:14> - Input Divider settings. Bits <25:22> - Lock-detect window width. “0000” = Narrow window, “0001”, “0010”,”0100”,”0101”, ... 1110” = Widest window, “XX11” = Reserved. Bit <26> - “0” = triggers after first lock detection, “1” = triggers after 64 cycles of lock detection. Bit <27> - “0” selects digital PLL_Lock 0, “1” selects digital PLL_Lock 1.
Control Register 6	0xB8	32	Bit <0> - VCO select, “0”: VCO1 (low range), “1”: VCO2 (high range). Bits <2:1> - Pre-scaler setting. Bits <23, 11> - Reserved, must be set to “0”. Bits <15:13> - Bypass Divider setting. Bits <10:3> - Feedback Divider setting. Bit <26> - “1” = External loop filter is used, “0” = Internal loop filter is used. Bit <12> - “0” = Secondary input buffer internal termination enabled, “1” = Secondary internal termination circuitry disabled. Bit <20> - “0” = outputs synchronized to reference input on low-to-high pulse on SYNC pin, “1” = outputs synchronized to SYNC high-to-low pulse. Bit <21> - “1” = Wide pulse, “0” = Narrow pulse. Bit <22> - Enable VCO calibration command. Bit <24> - Enable auxiliary output when set to “1”. Bit <25> - Select the output that will drive AUX output. “0” = Output divider 2, “1” = divider 3. Bit <27> - “1”: Calibration mode = Manual mode, “0”: Calibration mode = startup mode. Bits <19:16> - Charge Pump current select.
Control Register 7	0xBC	32	Bits <20:0> - Loop filter control setting. Bit <21> - Reserved, must be set to “0”. Bits <24, 22> - Diagnostics, set to “1”. Bits <25, 23> - Smart Mux. “0” enables short delay for fast operation, “1” for long delay. Bit <26> - Read only. “0” = EEPROM unlock. “1” = EEPROM locked. Bit <27> - Reserved, always reads “1”.

Registers: Clock Driver cont.

Register	Address	Data Width	Description
Control Register 8	0xC0	32	Bits <5:0> - Calibration read back from device. Bit <6> - Read only, status of the PLL lock pin driven by the device. Bit <7> - "0" = Set device Sleep mode ON, "1" = Normal mode. Bit <8> - "0" = Forces /SYNC, "1" = exit Sync. Bits <20, 13, 9> - Reserved, must be set to "0". Bits <12:10> - Silicon Revision. Bits <24:21, 19:14> - Factor registers. Bits <27:24> - Synthesizer Source Indicator.
Unlock CDCE62005	0xC4	8	Write Only. Bit <0> - Unlock CDCE62005.
Lock CDCE62005	0xC5	8	Write Only. Bit <0> - Copy data from RAM to EEPROM. Use discouraged.
Oscillator Enable	0xC6	8	Bit <0> - "1" – Enable internal oscillator for ADC clock.
Clock Reference Select	0xC7	8	Bit <0> - By pin, optional to SPI
Clock Base SYNC	0xC8	8	Bit <0> - By pin, optional to SPI
Clock Base Power Down	0xC9	8	Bit <0> - By pin, optional to SPI
Clock Base PLL Lock	0xCA	8	Bit <0> - "1" – PLL locked.

Registers: Flash

Register	Address	Data Width	Description
Write Enable	0x160	8	Write command to enable write ops to Flash.
Write Disable	0x161	8	Write command to disable write ops to Flash.
Read/Write Status	0x162	8	Read/Write to Flash status register.
Erase Bulk	0x163	8	Write command to erase bulk in Flash.
Read Flash Chip ID	0x164	8	Read Flash ID.
Erase Sector	0x168	32	Write command to erase sector of Flash. Bits <23:0> - Number of sectors.

Registers: Remote Update

Register	Address	Data Width	Description
Read Master State Machine (MSM) Current State Mode	0x180	8	NA
Read Past Status 1 MSM Mode	0x181	8	NA
Read Current Application Mode Watch Dog Enable	0x182	8	NA
Read Past Status 1 Reconfiguration Trigger Conditions Source	0x183	8	NA
Read Past Status 2 MSM Mode	0x184	8	NA
Read Past Status 2 Reconfiguration Trigger Conditions Source	0x185	8	NA
R/W the Early Conf_Done Check	0x186	8	NA
R/W Watchdog Enable Value	0x187	8	NA
R/W The Osc_Internal Option	0x188	8	NA
R/W Watchdog Timeout Value	0x18A	16	NA
Read Current Application Mode Watchdog Time Value	0x18C	32	NA
Read Past Status 1 Boot Address	0x190	32	NA
Read Past Status 2 Boot Address	0x194	32	NA
R/W Boot Address (Upper 22 bits of 24 bit address value)	0x198	32	NA
Read Current Factory Mode Boot Address 24 bit	0x19C	32	NA
Write the Command to Reconfigure FPGA	0x1A0	8	NA
Write the Command to Reset Watchdog Timer	0x1A6	8	NA